

Serial No.: 09/891,999  
Examiner: Phan, Raymond Ngan

**REMARKS/ARGUMENTS**

Claims 1-33 are pending.

The title has been changed in response to the Examiner's request, in order to be more descriptive of the invention.

[re Office Action Section 5]

Claims 1-5 have been rejected under 35 USC 102(b) as being anticipated by Cherukuri (US 5,878,217). Applicant respectfully traverses.

Claim 1 requires "a first memory interface disposed between said first interface controller and a memory block" and "a second memory interface disposed between said memory block and said second interface controller". The circuit designated by the Examiner as first interface (10Base-I Interface 114) is not disposed between the circuit designated by the Examiner as first interface controller (Media Access Controller 110) and the designated memory block (Buffer and Storage Arrays 102). Further, the circuit designated by the Examiner as second interface (Host Bus Interface 118) is not disposed between the circuit designated by the Examiner as second interface controller (DMA Logic and Transport Controller 120) and the designated memory block (Buffer and Storage Arrays 102). Accordingly, it is submitted that Claims 1-5 are not anticipated by Cherukuri.

Moreover, the difference in structure between Applicants' invention and the system of Cherukuri serve to emphasize that the structures are for different purposes, solving different problems. It is submitted that there is nothing in Cherukuri to suggest or render obvious the card and systems of Applicants.

With respect to claim 2, Applicants respectfully disagree with the Examiner that Cherukuri shows "a network interface coupled to a switch fabric disposed in a telecommunications node". Applicants have repeatedly reviewed the section to which the Examiner has drawn attention and find nothing about a switch matrix. The term "switch" is found in connection with DMA Switch Control Logic of Fig. 3 in Cherukuri, but this is a switching between two different transfer modes (column 6, line 33), not a switch matrix.

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Likewise, as required by claim 3, there is no Ethernet switch fabric disclosed in Cherukuri.

With respect to claim 4, Applicants do not find a mention of error correction in Cherukuri.

Accordingly, it is submitted that claims 1 and claims 2-5 dependent thereon are not anticipated by Cherukuri, and it is further submitted that the invention of such claims is not obvious in view of Cherukuri.

[re Office Action Section 7]

Claims 6-8 are rejected under 35 USC 103(a) as unpatentable over Cherukuri in view of Matsushima et al.(US 5,706,482).

For the reasons given above, it is submitted that claim 1 is not obvious in view of Cherukuri. Further it is submitted that there is no suggestion of the structure of claim 1 in Cherukuri taken together with the description of DRAM and SRAM by Matsushima. Accordingly, it is submitted that claim 1 and claims 6-8 dependent thereon are not obvious in view of Cherukuri in view of Matsushima

[re Office Action Section 8]

Claims 9-11 are rejected under 35 USC 103(a) as unpatentable over Cherukuri in view of Matsushima and Lanus et al. (US 6,112,271).

For the reasons given above, it is submitted that claim 1 is not obvious in view of Cherukuri in view of Matsushima. Further it is submitted that there is no suggestion of the structure of claim 1 in Cherukuri and Matsushima taken together with the description by Lanus et al. of a multiconfiguration backplane with COMPACTPCI Bus. Accordingly, it is submitted that claim 1 and claims 9-11 dependent thereon are not obvious in view of Cherukuri in view of Matsushima and Lanus et al.

[re Office Action Section 9]

Claims 12-16, 20-21, 24-26, 32-33 have been rejected under 35 USC 103(a) as unpatentable over Velamuri et al. (US 6,286,011) in view of Cherukuri.

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The Examiner states that Velamuri does not disclose "at least one memory card disposed in a system shelf forming a portion of said telecommunications node, said at least one memory card cooperating with a network interface for receiving said database update signals through a switch fabric, wherein said at least one memory card is operable to contain at least a portion of said distributed database in a memory block disposed thereon", but that it would be obvious to combine the teachings of Cherukuri within the system of Velamuri et al.

However, Cherukuri also does not disclose "receiving said database update signals through a switch fabric". Accordingly, it is submitted that the combination of the references Velamuri et al. and Cherukuri does not show or render obvious the invention described by claims 12 and 24, and claims 13-16, 20-21, 25-26, and 32-33 dependent thereon.

[re Office Action Section 10]

Claims 17-19, 27-29 have been rejected under 35 USC 103(a) as unpatentable over Velamuri et al. in view of Cherukuri and further in view of Matsushima et al.

For the reasons given above, it is submitted that claims 12 and 24 are not obvious in view of Velamuri in view of Cherukuri. Further it is submitted that there is no suggestion of the structure of claims 12 and 24 in Velamuri and Cherukuri taken together with the description by Matsushima of DRAM and SRAM. Accordingly, it is submitted that claims 12 and 24 and claims 17-19, 27-29 dependent thereon are not obvious in view of Velamuri et al. in view of Cherukuri and further in view of Matsushima et al.

[re Office Action Section 11]

Claims 21-23, 30-31 have been rejected under 35 USC 103(a) as unpatentable over Velamuri et al. in view of Cherukuri and further in view of Lanus et al.

For the reasons given above, it is submitted claims 12 and 24 are not obvious in view of Velamuri in view of Cherukuri. Further it is submitted that there is no suggestion of the structure of claims 12 and 24 in Velamuri and Cherukuri taken together with the description by Lanus et al. of a multiconfiguration backplane with COMPACTPCI Bus. Accordingly, it is submitted that 12 and 24 and claims 21-23, 30-31 dependent thereon are not obvious in view of Velamuri et al. in view of Cherukuri and Lanus et al.

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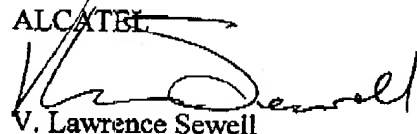
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It is believed that the foregoing amendment places the Application in condition for allowance; therefore, Applicant respectfully requests withdrawal of the Examiner's rejection of claims 1-33 and allowance of same. Should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned to expeditiously resolve any outstanding issues.

Respectfully submitted,

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